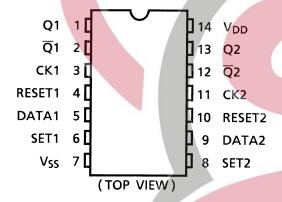
TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

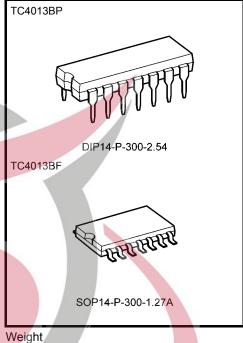
TC4013BP, TC4013BF

TC4013B Dual D-Type Flip Flop

TC4013B contains two independent circuits of D type flip-flop. The input level applied to DATA input are transferred to Q and \overline{Q} output by rising edge of the clock pulse. When SET input is placed at "H", and RESET input is placed at "L", outputs become Q = "H", and \overline{Q} = "L". When RESET input is placed at "H", and SET input is placed at "H", and SET input is placed at "L", outputs become Q = "H", and \overline{Q} = "H". When both of RESET input and SET input are at "H", outputs become Q = "H" and \overline{Q} = "H".

Pin Assignment

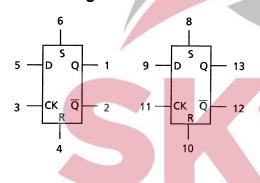




DIP14-P-300-2.54 : SOP14-P-300-1.27A :

: 0.96 g (typ.) : 0.18 g (typ.)

Block Diagram





Start of commercial production 1985-02

Truth Table

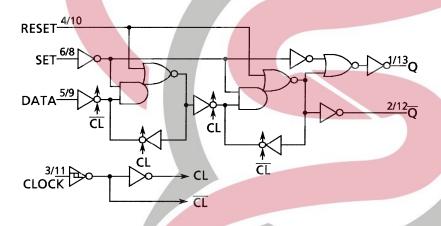
	Inp	Outputs				
RESET	SET	DATA CKA		Qn + 1	Q n + 1	
L	Н	*	*	Н	L	
Н	L	*	*	L	Н	
Н	Н	*	*	Н	Н	
L	L	L		L	Н	
L	L	Н		Н	L	
L	L	*		Qn [·]	- Qn	

*: Don't care

Δ: Level change

·: No change

Logic Diagram



Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
DC supply voltage	V_{DD}	V _{SS} - 0.5 to V _{SS} + 20	V
Input voltage	V _{IN}	V _{SS} – 0.5 to V _{DD} + 0.5	V
Output voltage	V _{OUT}	$V_{SS} - 0.5$ to $V_{DD} + 0.5$	V
DC input current	I _{IN}	±10	mA
Power dissipation	PD	300 (DIP)/180 (SOP)	mW
Operating temperature range	T _{opr}	-40 to 85	°C
Storage temperature range	T _{stg}	-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).



Operating Ranges (V_{SS} = 0 V) (Note)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
DC supply voltage	V_{DD}	_	3	_	18	V
Input voltage	V _{IN}	_	0	_	V_{DD}	V

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{DD} or V_{SS} .

Static Electrical Characteristics ($V_{SS} = 0 V$)

Characteristics Symbol		Svm-	Test Condition		-40°C		25°C			85°C		11-4
			V _{DD}	Min	Max	Min	Тур.	Max	Min	Max	Unit	
			I _{OUT} < 1 μA V _{IN} = V _{SS} , V _{DD}	5	4.95	_	4.95	5.00		4.95	_	
High-level output voltage	V _{OH}	10		9.95	-	9.95	10.00	-	9.95	_	V	
			VIN - VSS, VDD	15	14.95		14.95	15.00	-	14.95	_	
			I _{OUT} < 1 μA	5	_	0.05	_	0.00	0.05	_	0.05	
Low-level or voltage	utput	V_{OL}	$V_{IN} = V_{SS}, V_{DD}$	10		0.05		0.00	0.05	_	0.05	V
			VIIV = \$35, \$DD	15	_	0.05	_	0.00	0.05	_	0.05	
			V _{OH} = 4.6 V	5	-0.61	_	-0.51	-1.0	-	-0.42	_	
			V _{OH} = 2.5 V	5	-2.50	_	-2.10	-4.0	-	-1.70	_	mA
Output high	current	Іон	V _{OH} = 9.5 V	10	-1.50	_	-1.30	-2.2	_	-1.10	_	
			V _{OH} = 13.5 V	15	-4.00	-	-3.40	-9.0	+	-2.80		
			$V_{IN} = V_{SS}, V_{DD}$									
		l _{OL}	V _{OL} = 0.4 V	5	0.61		0.51	1.2	/-	0.42	_	mA
Output low of	current		V _{OL} = 0.5 V	10	1.50	_	1.30	3.2	_	1.10	_	
Catpution	ouron		V _{OL} = 1.5 V	15	4.00		3.40	12.0	_	2.80	4-1	
			$V_{IN} = V_{SS}, V_{DD}$									
		VIH	V _{OUT} = 0.5 V, 4.5 V	5	3.5		3.5	2.75	_	3.50		٧
Input high v	roltage		V _{OUT} = 1.0 V, 9.0 V	10	7.0	_	7.0	5.50	_	7.00	_	
mpat mgm v	onago /		V _{OUT} = 1.5 V, 13.5 V	15	11.0	_	11.0	8.25	_	11.00	_	
			I _{OUT} < 1 μA									
			V _{OUT} = 0.5 V, 4.5 V	5	-/-	1.5		2.25	1.5		1.5	
Input low voltage	V _{IL}	V _{OUT} = 1.0 V, 9.0 V	10	\mathcal{L}	3.0		4.50	3.0		3.0	V	
		V _{OUT} = 1.5 V, 13.5 V	15	-	4.0	_	6.75	4.0		4.0		
		$ I_{OUT} < 1 \mu A$		E			TE	0.0				
iliput	"H" level	Чн	V _{IH} = 18 V	18		0.1		10 ⁻⁵	0.1		1.0	μА
current "	"L" level	I _I L	V _{IL} = 0 V	18	_	-0.1	_	-10^{-5}	-0.1	_	-1.0	μιτ
			V V	5	_	1	_	0.002	1	_	30	
Quiescent s current	Quiescent supply current		$V_{IN} = V_{SS}, V_{DD}$ (Note)	10	_	2	_	0.004	2	_	60	μΑ
			(1315)	15	_	4	—	0.008	4	—	120	

Note: All valid input combinations.

TC4013BP/BF

Dynamic Electrical Characteristics (Ta = 25°C, V_{SS} = 0 V, C_L = 50 pF)

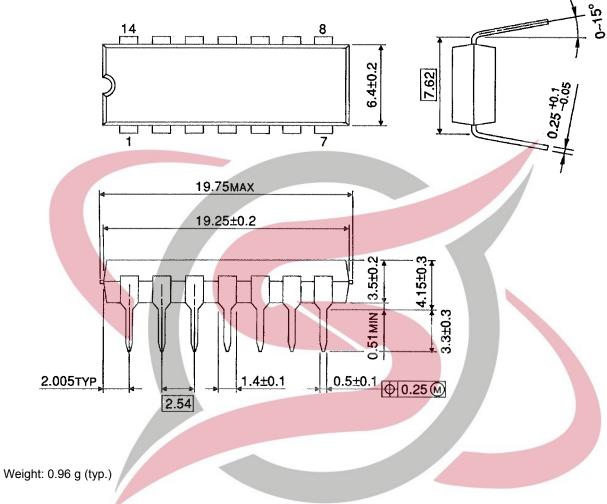
Ch arrastariation	Symbol	Test Condition	Min	T	Mari	Unit	
Characteristics	Symbol		V _{DD} (V)	Min	Тур.	Max	Unit
Output transition time			5	_	70	200	
(low to high)	t _{TLH}	_	10	_	35	100	ns
(low to riigit)			15	_	30	80	
Output transition time			5	_	70	200	
(high to low)	t _{THL}	_	10	_	35	100	ns
(night to low)			15	_	30	80	
Propagation delay time	tauu		5	_	130	300	
(CK-Q, \overline{Q})	t _{pLH}	_	10	_	65	130	ns
(OR-Q, Q)	t _{pHL}		15	_	50	90	
Propagation delay time			5	-/	110	300	
(SET, RESET-Q, \overline{Q})	t _{pLH}	_	10	-4	50	130	ns
(OET, NEOET W, W)			15	4	40	90	
Propagation delay time			5	7	110	300	
(SET, RESET-Q, $\overline{\mathbb{Q}}$)	t _{pHL}	<u> </u>	10	_	50	130	ns
(OET, NEOET-Q, Q)			15	<u></u>	40	90	
			5	3.5	8	_	
Max clock frequency	f _{CL}	-	10	8.0	16	_	MHz
			15	12.0	20	_	
Max clock input rise time	t _{rCL}		5				
Max clock input fall time	t _{fCL}	_	10		No limit		μS
max order input fair time	HOL		15		r		
Min pulse width			5	_	60	180	
(SET, RESET)	t _W	_	10	_	30	80	ns
			15	_	25	50	
			5	_	60	140	
Min clock pulse width	t _W	_	10	_	30	60	ns
			15	_	25	40	
Min set-up time			5	_		40	
(DATA-CK)	t _{su}		10	_		20	ns
			15	_		15	
Min hold time			5	_	20	40	
(DATA-CK)	t _H	ELEC	10	R • O	10	20	ns
			15	_	6	15	
Min removal time			5	-	_	40	
(SET, RESET-CK)	t _{rem}	_	10	_	_	20	ns
			15		_	15	
Input capacitance	C _{IN}	_		_	5	7.5	pF

Waveform for Measurement of Dynamic Characteristics

Waveform 1 20ns 20ns 90% 90% **DATA** 50% 50% 50% 10% 10% t_H 20ns 20ns 90% -90% **CLOCK** 50% 50% 10% 10% 90% 90% Q 50% 50% 10% - 10% t_{PLH} t_{PHL} Waveform 2 20ns 20ns 90% 90% SET 50% 50% 10% 10% 20ns 20ns 90% 90% RESET 50% 50% 10% 10% tw 50% - 50% t_{PHL}

Package Dimensions

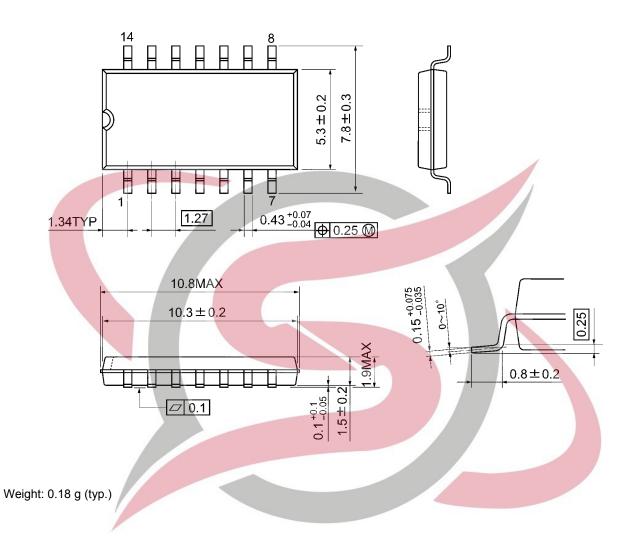
DIP14-P-300-2.54 Unit: mm



LECTRO

Package Dimensions

SOP14-P-300-1.27A Unit: mm





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